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09/274,430	03/22/1999	MICHAEL BARROW	042390.P3495	8388

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EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/274,430	Applicant(s) BARROW, MICHAEL
	Examiner John B. Vigushin	Art Unit 2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *40-44* is/are allowed.

6)☒ Claim(s) *17,18,20-22,24-31,33-38 and 45-51* is/are rejected.

7)☒ Claim(s) *19,23,32 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *17 & 22* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on May 24, 2002 (Certificate of Mailing date: May 21, 2002) has been entered.

Claim Objections

2. Claim 45 is objected to because of the following informalities:

In line 3: --a-- should be inserted after "having".

In line 5: "contacts" should be changed to --contact--.

In line 12: "substate" should be changed to --substrate--.

Appropriate correction is required.

Rejections Based On Prior Art

3. The following references were relied upon for the rejections hereinbelow:

1) Rostoker et al. (US 5,729,894) 2) Suyama et al. (US 5,731,630)

*3) *Electronic Design* Magazine, publ. February 06, 1995, the article *Plastic Ball-Grid Arrays Continue to Evolve*, on pp.141-146.

*4) *Semiconductor Group Package Outlines*: Reference Guide, publ. 1995 by Texas Instruments (Plastic Ball Grid Array Drawings).

*Made of record in Applicant's IDS of May 24, 2002 (filed as Paper No. 22 in the instant Application).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 17, 18, 20-22, 24, 25, 30, 31, 33, 34, 37 and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by Rostoker et al.

As to Claim 17, Rostoker et al. discloses, in Fig. 12: a substrate 506 with a top surface, and an exposed external opposite (bottom) surface 516; the bottom surface defined by a first region (i.e., the central area defined within the imaginary line 508), a

second region (around the periphery of imaginary line 508 and exterior to the first region defined by the imaginary line 508), and a third region (which includes the imaginary line 508 and the non-contact space on each side of line 508) that separates the first and second regions; a first plurality of contacts (corresponding to bumps 520; the contacts--i.e. "contact sites"--beneath the bumps will be referenced hereinafter by the bump reference number "520" for convenience; col.4: 52-57) located in the second (peripheral) region and a second plurality of contacts 520 located in the first (central) region such that a smallest distance between adjacent contacts in the first region (i.e., 0.050 inches; col.7: 56-59) is different than a distance between the first and second regions (i.e., the "width" of the third region which is also the distance between the adjacent contacts in the second region, i.e., 0.100 inches; col.7: 59-61), wherein the third region does not have any contacts located therein (see Fig. 12), as noted above.

As to Claim 18, Rostoker et al. further discloses that the smallest distance between adjacent contacts in the first region--i.e., 0.050 inches--is smaller than the distance between the first and second regions--i.e., 0.100 inches--(Fig. 12; col.7: 56-61).

As to Claim 20, Rostoker et al. further discloses that package 500 is a BGA package (Fig. 12; col.7: 29-30).

As to Claim 21, Rostoker et al. further discloses that the plurality of contacts 520 include a plurality of contact pads (as noted above, in the rejection of base Claim 17, this is best disclosed in Fig. 4 and the "contact sites" in col.4: 52-57).

As to Claim 22, Rostoker et al. further discloses a plurality of solder balls attached to the contact pads (col.4: 55-57).

As to Claim 24, Rostoker et al. further discloses that the plurality of contacts ("contact sites") are located on the exposed external opposite (bottom) surface of substrate 506 (again, as indicated in base Claim 17, best seen in Fig. 4 and col.4: 52-56).

As to Claim 25, Rostoker et al. further discloses that the top surface of substrate 506 has a plurality of bond pads (best seen in the bond pads 208 of the embodiment of Fig. 4, upon which embodiment--Figs. 4-6--the embodiment of Fig. 12 is based; Fig. 4 and col.4: 44-49).

As to Claim 30, Rostoker et al. discloses, in Fig. 12: a substrate 506 having a plurality of bond pads and an IC mounted to the top surface of substrate 506 and coupled to the bond pads 208 (the IC and bond pads are not shown in Fig. 12 which is an alternate embodiment of the exposed (bottom) surface of Fig. 6 corresponding to the Fig. 4 embodiment; accordingly, the bond pads and IC of Fig. 12 are best seen in the bond pads 208 and IC 202 of Fig. 4); substrate 506 also includes an exposed external opposite (bottom) surface 516 defined by an inner region (the central area defined within the imaginary line 508), an outer region (around the periphery of imaginary line 508 and exterior to the central area defined by the imaginary line 508), and a middle region (which includes the imaginary line 508 and the contact-free space on each side of line 508) that separates the inner and outer regions; a first plurality of contacts (corresponding to bumps 520; the contacts--i.e. "contact sites"--beneath the bumps will

be referenced hereinafter by the bump reference number "520" for convenience; col.4: 52-57) located in the outer region and a second plurality of contacts 520 located in the inner region such that a first smallest distance (0.050 inches) between adjacent contacts in the inner region (col.7: 56-59) is different than a second smallest distance between the inner and outer regions (i.e., the "width" of the third region which is also the distance between the adjacent contacts in the outer region, i.e., 0.100 inches; col.7: 59-61), wherein the middle region is free of contacts (see Fig. 12), as noted above.

As to Claim 31, Rostoker et al. further discloses that the first smallest distance--i.e., 0.050 inches--is smaller than the second smallest distance--i.e., 0.100 inches--(Fig. 12; col.7: 56-61).

As to Claim 33, Rostoker et al. further discloses that package 500 is a BGA package (Fig. 12; col.7: 29-30).

As to Claim 34, Rostoker et al. further discloses a plurality of solder balls attached to the contacts (col.4: 55-57).

As to Claim 37, Rostoker et al. further discloses that the IC is enclosed by an encapsulant (best seen in the Fig. 4 embodiment, wherein IC 202 is enclosed by encapsulant 226).

As to Claim 38, Rostoker et al. further discloses that the first (peripheral) plurality of contacts 520 is located outside an outer dimensional profile of the IC (compare the bottom surface contact arrays 220 and 520 with respect to IC 202 as shown in the related embodiments in Figs. 4 and 12).

6. Claims 45-48, 50 and 51 are rejected under 35 U.S.C. 102(e) as being anticipated by Suyama et al.

As to Claim 45, Suyama et al. discloses, in Figs. 1, 2 and 4: a substrate 100 that has a top surface and an exposed external opposite bottom surface; the external bottom surface having a plurality of contact pads 10 and 11; the plurality of contact pads 10 and 11 consisting only of: an outer array of contact pads 10,each of the contact pads 10 separated from each other by a first distance (i.e., the distance between adjacent vias 5 which correspond to contacts 10, as best seen in Figs. 1 and 2); a center array of contact pads 11, each of contact pads 11 separated by a second distance (i.e., the distance between adjacent vias 6 which correspond to contacts 11, as best seen in Figs. 1 and 2); the center array of contact pads 11 being separated from the outer array of contact pads 10 by a third distance (i.e., the distance--even the shortest one--between vias 5 and 6 corresponding to contacts 11 and 10, respectively) which is larger than the first and second distances (Fig. 1); a plurality of solder balls attached to contact pads 10 and 11 (Figs. 2 and 4; col.3: 27-32).

As to Claim 46, Suyama et al. further discloses that the outer array of contact pads 10 is located outside an outer dimensional profile of an IC 8 coupled to the top surface of substrate 100 (col.4: 11-12; compare Figs. 1 and 4: contact pads 10 are located at the periphery of substrate 100, well outside of the outer dimensional profile of IC 8).

As to Claim 47, Suyama et al. further discloses that the center array of contact pads 11 is located inside the outer dimensional profile of an IC 8 coupled to the top

surface of substrate 100 (col.4: 11-12; compare Figs. 1 and 4: contact pads 10 are located in the area defined within the openings 3 in substrate 100, and therefore are well within the outer dimensional profile of IC 8).

As to Claim 48, Suyama et al. further discloses that the outer array of contact pads 10 is located outside an outer dimensional profile of an IC 8 coupled to the top surface of substrate 100 (col.4: 11-12; compare Figs. 1 and 4: contact pads 10 are located at the periphery of substrate 100, well outside of the outer dimensional profile of IC 8); and that the center array of contact pads 11 is located inside the outer dimensional profile of an IC 8 coupled to the top surface of substrate 100 (col.4: 11-12; compare Figs. 1 and 4: contact pads 10 are located in the area defined within the openings 3 in substrate 100, and therefore are well within the outer dimensional profile of IC 8).

As to Claim 50, Suyama et al. further discloses that the smallest distance between adjacent contact pads 10 in the outer array is smaller than the distance (even the shortest distance) between the outer array of contact pads 10 and the center array of contact pads 11 (Fig. 1).

As to Claim 51, Suyama et al. further discloses that the top surface of substrate 100 has a ground bus (disclosed but not shown; col.5: 1-3) that is connected to the center array 11 of contact pads by a plurality of vias 6 that extend through substrate 100 (Figs. 1 and 4; col.5: 1-8).

7. Claims 17, 18, 20-25, 29, 45, 47, 49 and 50 are rejected under 35 U.S.C. 102(b) as being anticipated by *Semiconductor Group Package Outlines*, Reference Guide,

published by Texas Instruments (TI) in 1995 (hereinafter referred to as "the TI Reference Guide").

Examiner's Note: The TI Reference Guide provides only the year of publication (1995); but the drawings are dated as October 1994 on p.6-20 of the document. Therefore, the Examiner believes he is justified in assuming that this document has been published early enough in 1995 to pre-date the Applicant's 131 Affidavit date which is generally indicated as April 1995 (see Paper No. 8 filed on December 07, 2000 in the instant Application). Unless the Applicant establishes that this document is not a 102(b) document, the Examiner will consider the TI Reference Guide as a 102(b) reference, as applied to the rejections below.

As to Claim 17, the TI Reference Guide discloses, in the three drawings on p.6-20: a substrate that has a top surface and an exposed external opposite (bottom) surface defined by a first (central) region, a second (outer) region, and a third (non-contact) region that separates the first and second regions; a plurality of contacts including a first plurality of contacts located in the second (outer) region, and a second plurality of contacts located in the first (central) region such that a smallest distance between adjacent contacts in the first (central) region is different than a distance between the first and second regions, wherein the third region does not have any contacts located therein.

As to Claim 18, the TI Reference Guide further discloses, in the three drawings on p.6-20, that the smallest distance between adjacent contacts in the first region is smaller than the distance between the first and second regions.

As to Claim 20, the TI Reference Guide further discloses, in the three drawings on p.6-20, that the semiconductor package is a ball grid array package (i.e., a Plastic Ball Grid Array).

As to Claim 21, the TI Reference Guide further discloses, in the three drawings on p.6-20, that the plurality of contacts comprises a plurality of contact pads.

As to Claim 22, the TI Reference Guide further discloses, in the three drawings on p.6-20, a plurality of solder balls attached to the contact pads.

As to Claim 23, the TI Reference Guide further discloses, in the three drawings on p.6-20, that the second plurality of contacts (i.e., the plurality of central contacts) is contained within a dimensional profile of an IC coupled to the top surface of the substrate.

As to Claim 24, the TI Reference Guide further discloses, in the three drawings on p.6-20, that the plurality of contacts is located on the exposed external opposite surface of the substrate.

As to Claim 25, the top surface of the substrate inherently has a plurality of bond pads for connection to the IC terminals in the package disclosed in the three drawings on p.6-20 of the TI Reference Guide.

As to Claim 45, the TI Reference Guide discloses, in the three drawings on p.6-20: a substrate that has a top surface and an exposed external bottom surface, the external bottom surface having a plurality of contact pads, the plurality of contact pads consisting only of: an outer array of contact pads, each of the contact pads separated from each other by a first distance; a center array of contact pads, each of the contact

pads separated by a second distance, the center array of contact pads being separated from the outer array of contact pads by a third distance which is larger than the first and second distances.

As to Claim 47, the TI Reference Guide discloses, in three drawings on p.6-20, that the center array of contact pads is located inside the outer dimensional profile of an IC couple to the top surface of the substrate.

As to Claim 49, the TI Reference Guide discloses, in three drawings on p.6-20, that a distance between adjacent contact pads in the outer array is the same as the distance between adjacent contact pads in the center array.

As to Claim 50, the TI Reference Guide discloses, in three drawings on p.6-20, that the smallest distance between adjacent contact pads in the outer array is smaller than the distance between the outer array of contact pads and the center array of contact pads.

8. Claims 17, 18, 20-22, 24-27, 30, 33-35, 37 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by *Electronic Design*, published February 06 1995, the article by Jonathan L. Houghten on pp.141-146.

As to Claim 17, *Electronic Design* (article by Jonathan L. Houghten) discloses, in Fig. 3 on p.144: a substrate (the 256-lead plastic ball grid array on the right-hand side) including a top surface and an exposed external (bottom) surface (as shown in Fig. 3 on p.144) defined by a first (central) region, a second (outer) region, and a third (non-contact) region that separates the first and second regions; a first plurality of contacts located in the second (outer perimeter) region and a second plurality of contacts located

in the first (central) region (p.142, the full paragraph in col.2) such that a smallest distance between adjacent contacts in the first (central) region is different than a distance between the first and second regions, wherein the third region, as noted above, does not have any contacts therein (Fig. 3 on p.144).

As to Claim 18, the Houghten article further discloses that the smallest distance between adjacent contacts in the first (central) region is smaller than the distance between the first and second regions.

As to Claim 20, the Houghten article further discloses that the semiconductor package is a ball grid array (BGA) package (Fig. 3 on p.144).

As to Claims 21 and 22, the Houghten article further discloses that the plurality of contacts comprises a plurality contact pads for attaching the balls of the BGA (p.141, col.2: last seven lines-col.3: first two lines).

As to Claim 24, the Houghten article further discloses that the plurality of contacts is located on the exposed external opposite (bottom) surface of the substrate (p.144, Fig. 3).

As to Claim 25, the Houghten article further discloses that the top surface of the substrate as a plurality of bond pads (Fig. 1 on p.141).

As to Claim 26, the Houghten article further discloses that the top surface of the substrate has a ground bus connected to the second (central) plurality of contacts by a plurality of vias that extend through the substrate (p.142, the full paragraph in col.2).

As to Claim 27, the Houghten article further discloses that the first (peripheral) plurality of contacts comprises at least five rows of contacts (Fig. 3 on p.144 shows a section of the first plurality of contacts having five rows).

As to Claim 30, Electronic Design (article by Jonathan L. Houghten) discloses, in Fig. 3 on p.144: a substrate (the 256-lead plastic ball grid array on the right-hand side) including a top surface having a plurality of bond pads (Fig. 1 on p.141) and an exposed external (bottom) surface (as shown in Fig. 3 on p.144) defined by an inner (central) region, an outer region, and a middle (contact free) region that separates the inner and outer regions; a first plurality of contacts located in the outer region and a second plurality of contacts located in the inner (central) region (p.142, the full paragraph in col.2) such that a first smallest distance between adjacent contacts in the inner (central) region is different than a second smallest distance between the inner and outer regions, wherein the middle region, as noted above, is a contact free region (Fig. 3 on p.144).

As to Claim 33, the Houghten article further discloses that the semiconductor package is a ball grid array (BGA) package (Fig. 3 on p.144).

As to Claim 34, the Houghten article further discloses a plurality of solder balls attached to the plurality of contacts (Fig. 3 on p.144; and p.141, col.2: last seven lines-col.3: first two lines).

As to Claim 35, the Houghten article further discloses that the top surface of the substrate has a ground bus connected to the second (central) plurality of contacts by a plurality of vias that extend through the substrate (p.142, the full paragraph in col.2).

As to Claim 37, the Houghten article further discloses that the IC is enclosed by an encapsulant (Fig. 1 on p.141).

As to Claim 38, the Houghten article further discloses that the first (outer) plurality of contacts is located outside an outer dimensional profile of the IC (Fig. 1 on p.141 and Fig. 3 on p.144).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Semiconductor Group Package Outlines*, Reference Guide, published by Texas Instruments (TI) in 1995 (hereinafter referred to as "the TI Reference Guide").

The TI Reference Guide discloses, in three drawings on p.6-20, that the second plurality of contacts is arranged in a five by five matrix, but does not teach a four by four matrix arrangement.

Since it is old and well-known in the art to mount a BGA to a system circuit board, then would have been an obvious matter of engineering choice to modify the second (central) plurality of contacts (and, for that matter, the layout of the first plurality of contacts, as well) in accordance with the connection requirements of the system board, including modifying the disclosed five by five matrix to be a four by four matrix

instead, for connection to a particular system board that requires such a layout for mounting the BGA.

11. Claims 28 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Electronic Design*, published February 06 1995 (the article by Jonathan L. Houghten on pp.141-146), in view of Suyama et al.

As to Claims 28 and 36:

I. *Electronic Design* (article by Jonathan L. Houghten) teaches that the top surface of the substrate has a **ground** bus connected to the second (central) plurality of contacts by a plurality of vias that extend through the substrate (p.142, the full paragraph in col.2) but does not teach that the top surface of the substrate has a **power** bus connected to the second (central) plurality of contacts by a plurality of vias that extend through the substrate.

II. Suyama et al. discloses the top surface of the substrate has a ground bus and a power bus connected to the second (central) plurality of contacts by a plurality of vias that extend through the substrate; i.e., the top surface of substrate 100 has a ground bus (disclosed but not shown; col.5: 1-3) that is connected to the center array 11 of contact pads by a plurality of vias 6 that extend through substrate 100 for the purpose of shortening the electrical lengths between the ground and the IC 8, and between the power supply and the IC 8 in order to reduce parasitic inductance and power supply noise (Figs. 1 and 4; col.5: 1-8).

III. Since the article by Houghten and the patent awarded to Suyama et al. both teach BGA devices, the reduction of parasitic inductance and power supply noise, as

taught by Suyama et al. would have been readily recognized as beneficial to the package disclosed in Fig. 3 on p.144 of the package disclosed in the Houghten article (as evidenced by p.142, col.2: the full paragraph).

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further provide in Houghten, along with the disclosed ground bus, a power bus on the top surface of the substrate that is connected to the second (central) plurality of contacts by a plurality of vias that extend through the substrate in order to better reduce parasitic inductance and power supply noise in the package of Houghten, as taught by Suyama et al.

Allowable Subject Matter

12. Claims 40-44 have been allowed.

13. Claims 19, 23, 32 and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 19, patentability resides in *the smallest distance between adjacent contacts in the first region is larger than the distance between the first and second regions*, in combination with the other limitations of the claim.

As to Claim 23, patentability resides in that *each of the second plurality of contacts is contained within a dimensional profile of an integrated circuit coupled to the top surface of the substrate*, in combination with the other limitations of the claim.

As to Claim 32, patentability resides in *the first smallest distance is larger than the second smallest distance*, in combination with the other limitations of the claim.

As to Claim 39, patentability resides in that *the second plurality of contacts is located inside the outer dimensional profile of the integrated circuit*, in combination with the other limitations of the claim.

As to Claims 40-44, patentability resides in that *the first region is substantially equal to the dimensional profile of the integrated circuit*, in combination with the other limitations of base Claim 40.

15. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) The following references teach a substrate with a bottom surface having a central and an outer array of contacts:

Hamada et al. (US 5,324,985): contacts 6 in Fig. 1.

Andros et al. (US 5,367,435): contacts 51 in Figs. 1 and 2.

Davidson et al. (US 5,495,397): contacts 47 and 28 in Fig. 3.2.

Buckley, III et al. (US 5,477,082): inner and outer bumps on substrate 60 (Fig. 3).

Barber (US 5,895,968): inner contacts 412; outer contacts 416 (Fig. 4).

b) Hirano (US 5,309,024) discloses inner and outer contacts 12 and 13, respectively, on internal layers of a multilayer circuit (Figs. 20 and 21).

c) Selna (US 5,741,729) discloses sinking heat from IC 12 through the ground vias 6C (connected to ground plane 60) to bumps 14C, allowing IC 12 to operate at a lower package temperature (col.6: 50-61).

17. **Due to changes in the Office, the present Examiner has replaced Examiner David A. Foster as the Examiner of record**. Accordingly, any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
September 9, 2002